



MICROCIRCUIT DATA SHEET

MN54ABT16245-X REV 0B0

Original Creation Date: 10/16/95
Last Update Date: 09/14/98
Last Major Revision Date: 03/19/95

16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

General Description

The ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The TR inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

Industry Part Number

54ABT16245

NS Part Numbers

54ABT16245W-QML *

Prime Die

NB16245

Controlling Document

5962-9317502QXA*

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the ABT245
- A and B output sink capability of 48 mA, source capability of -24mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle.
- Non-Destructive hot insertion capability.

(Absolute Maximum Ratings)

(Note 1)

Vcc Pin Potential to Ground Potential	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30mA to +5.0mA
Voltage Applied To Any Output In the Disabled or Power-Off State In The High State	-0.5V to 5.5V -0.5V to Vcc
Current Applied To Output In The Low State (Max)	96mA
Junction Temperature (Tj) Ceramic	+175C
Thermal Resistance Junction-To-Case (Theta JC)	See Mil-Std 1835
Storage Temperature	-65C to +150C
Lead Temperature (Soldering, 10 seconds)	+300C
ESD Classification	Class 2
Maximum Power Dissipation	500 mW

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Supply Voltage (Vcc)	4.5V to 5.5V
Operating Temperature	-55C to +125C
Minimum Input Edge Rate (dV/dt) Data Input Enable Input	50 mV/ns 20 mV/ns
Maximum Output Current High Level (Ioh) Low Level (Iol)	-24 mA 48 mA

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICCH	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		2.0	mA	1, 2, 3
ICCL	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		60.0	mA	1, 2, 3
ICCZ	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		2.0	mA	1, 2, 3
ICCT	Supply Current per Input	VCC=5.5V, OE=0.0V Input under test=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		2.5	mA	1, 2, 3
		VCC=5.5V, OE=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		2.5	mA	1, 2, 3
		VCC=5.5V, OE=5.5V Input under test = 3.4V Other inputs = 5.5V or 0.0V	1, 4	VCC		50.0	uA	1, 2, 3
IIH	High Level Input Current	VCC=5.5V, VINH=5.5V	1, 4	IN		2.0	uA	1, 2, 3
IIL	Low Level Input Current	VCC=5.5V, VINL=0.0V	1, 4	IN		-2.0	uA	1, 2, 3
IOZH	Maximum TRI-STATE Leakage Current HIGH	VCC=5.5V, VOUT=2.7V VINL=0.0V, VIH (OE)=2.0V	1, 4	OUT		50.0	uA	1, 2, 3
IOZL	Maximum TRI-STATE Leakage Current LOW	VCC=5.5V, VOUT=0.5V VINH=5.5V, VIH (OE)=2.0V	1, 4	OUT		-50.0	uA	1, 2, 3
ICEX	Output High Leakage Current	VCC=5.5V, VOUT=5.5V VINH=5.5V	1, 4	OUT		50.0	uA	1, 2, 3
IOS	Output Short Circuit Current	VCC=5.5V, VOUT=0.0V VINH=5.5V	1, 4, 10	OUT	-100	-275	mA	1, 2, 3
IOS1	Output Short Circuit Current	VCC=5.5V, VOUT=2.5V VINH=5.5V	1, 4, 10	OUT	-50	-180	mA	1, 2, 3
IBVI	Input High Current Breakdown Test	VCC=5.5V, VINH=7.0V	1, 4	IN		7.0	uA	1, 2, 3
IZZ	Bus Drainage Test	VCC=0.0V, VOUT=4.5V, VINL=0.0V	1, 4	IN/OUT	-100	100	uA	1, 2, 3
VOL	Low Level Output Voltage	VCC=4.5V, IOL=48.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT		0.55	V	1, 2, 3

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VOH	High Level Output Voltage	VCC=4.5V, IOH=-24.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.0		V	1, 2, 3
		VCC=4.5V, IOH=-3mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.5		V	1, 2, 3
		VCC=5.0V, IOH=-3mA, VINH=5.0V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	3.0		V	1, 2, 3
VID	Input Leakage Test	VCC=0.0V, IID=1.9uA, VINL=0.0V	1, 4	IN	4.75		V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IKL=-18mA, VINH=4.5V, VINL=0.0V	1, 4	IN		-1.2	V	1, 2, 3
VOLP	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		0.9	V	4
VOLV	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		-1.4	V	4
VOHP	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		1.3	V	4
VOHV	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		-0.75	V	4
CIN	Input Capacitance	VCC=0.0V	7	IN		10.5	pF	4
COUT	Output Capacitance	VCC=5.0V	7	OUT		15.0	pF	4

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF RL=500 OHMS TRISE/TFALL = 3.0ns

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	An/Bn or Bn/An	0.5	4.3	ns	9
			2, 5	An/Bn or Bn/An	0.5	4.5	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V, VCC=4.5V & 5.5V @-55C/125C	2, 5	An/Bn or Bn/An	0.5	4.7	ns	9
			2, 5	An/Bn or Bn/An	0.5	5.2	ns	10, 11
tpZL	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	\overline{OE} to An or Bn	0.9	6.4	ns	9
			2, 5	\overline{OE} to An or Bn	0.9	6.9	ns	10, 11
tpZH	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	\overline{OE} to An or Bn	0.8	6.1	ns	9
			2, 5	\overline{OE} to An or Bn	0.8	6.4	ns	10, 11
tpHZ	Output Disable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	\overline{OE} to An or Bn	1.3	6.6	ns	9
			2, 5	\overline{OE} to An or Bn	1.3	6.9	ns	10, 11
tpLZ	Output Disable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	\overline{OE} to An or Bn	1.0	5.7	ns	9
			2, 5	\overline{OE} to An or Bn	1.0	6.9	ns	10, 11

Note 1: Screen tested 100% on each device at -55C, +25C & +125C Temp., Subgroups 1,2,3,7 & 8.

Note 2: Screen tested 100% on each device at -55C, +25C, and +125C temp., subgroups A9, A10, and A11.

Note 3: Screen tested 100% on each device at +25C temp. only, subgroup A9.

Note 4: Sample tested (Method 5005, Table 1) on each mfg. lot at +25C, +125C, & -55C temp. subgroups A1, 2, 3, 7 & 8.

Note 5: Sample tested (Method 5005, Table 1) on each mfg. Lot at +25C, +125C & -55C temp., subgroups A9, 10 & 11.

Note 6: Sample tested (Method 5005, Table 1) on each mfg. Lot at 25C temp only, subgroup A9.

Note 7: Not tested (Guaranteed by Design Characterization Data).

Note 8: Max number of outputs defines as (N). N-1 data inputs are driven 0V to 3V. one output @Vol or @Voh.

(Continued)

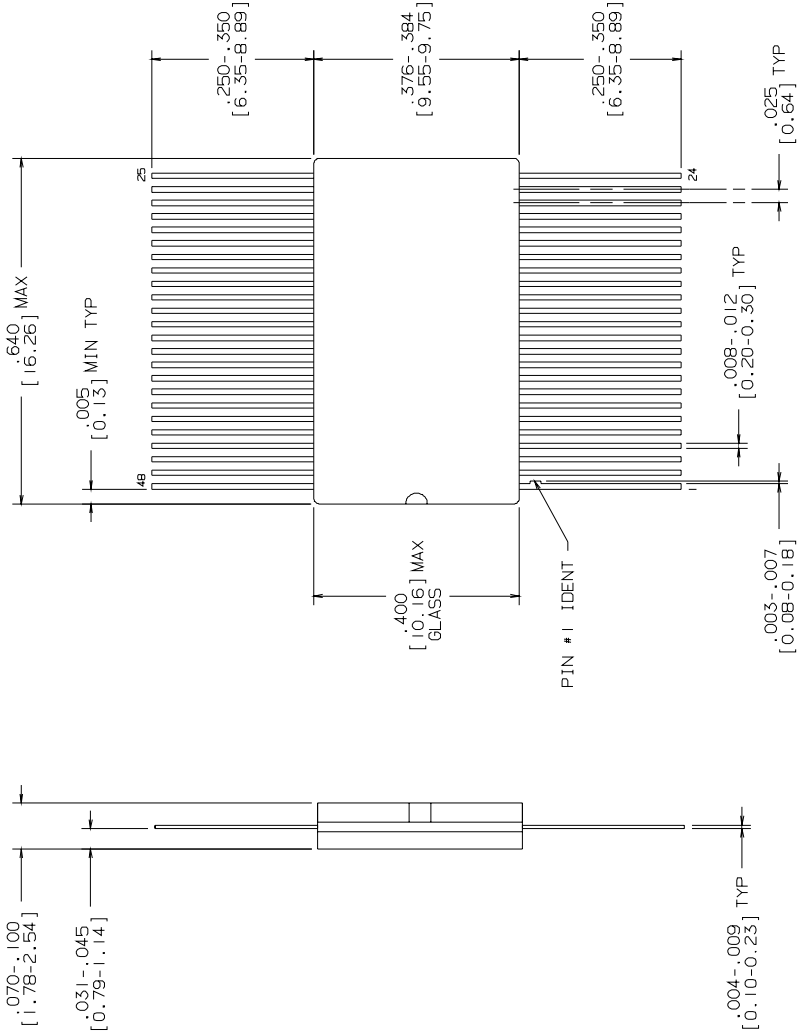
- Note 9: Max number of data inputs (N) switching. (N-1) inputs switching 0V to 3V.
Input-under-test switching : 3V to threshold (V_{ild}), 0V to threshold (V_{ihd}), Freq= 1
MHZ
- Note 10: Maximum test duration not to exceed one second, not more than one output shorted at
one time.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
WA48ARB	CERPACK, 48 LEAD, .025 LEAD PITCH (P/P DWG)

See attached graphics following this page.

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	09283	08/11/92
B	DIM .003-.007 [0.08-0.18] WAS .030-.045 [0.76-1.14] WAS .040-.054 [1.02-1.37]	09489	01/25/93
			M5/



MILAERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

- NOTES: UNLESS OTHERWISE SPECIFIED
- STANDARD LEAD FINISH: 200 MICRONS/5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 - THE LEAD FINISH, NICKEL UNDERPLATE, AND BASIS METAL SHALL CONFORM TO THE REQUIREMENTS OF MIL-M-38510.
 - REFERENCE JEDEC METRIC BALLLOT JC-11.10-92-75, ITEM 10-320, VARIATION AA, DATED JULY 9, 1992.

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN MARTA SUCHY	08/11/92
DFG: CHK.	
ENGR. CHK.	
APPROVAL	
NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
CERPAC, 48 LEAD, .025 LEAD PITCH	
SCALE	DRAWING NUMBER
N/A	C MKT-WA48A
REV	B
DO NOT SCALE DRAWING	
SHEET 1 OF 1	

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0001560	09/14/98	Bill Petcher	Change MDS MN54ABT16245-X REV 0A0 to MN54ABT16245-X REV 0B0