

**MN54ABT16500-X REV 0B0**

 Original Creation Date: 10/16/95  
 Last Update Date: 07/08/97  
 Last Major Revision Date: 04/18/97

**16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS**
**General Description**

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable(OEAB and /OEBA), latch-enable(LEAB and LEBA), and clock(/CLKAB and /CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if /CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of /CLKAB. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses /OEBA, LEBA and /CLKBA. The output enables are complementary (OEAB is active high and /OEBA is active low). To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

**Industry Part Number**

54ABT16500

**NS Part Numbers**

54ABT16500W-QML

**Prime Die**

NB6500

**Controlling Document**

See Features Page

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

Subgrp	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-Destructive hot insertion capability
- SMD : 5962-9687001-QXA

**(Absolute Maximum Ratings)**

Vcc Pin Potential to Ground Potential	-0.5V to +7.0V
Input Voltage	-0.5V to +7.0V
Input Current	-30mA to +5.0mA
Voltage Applied To Any Output	
In the Disabled or Power-Off State	-0.5V to 5.5V
In The High State	-0.5V to Vcc
Current Applied To Output	
In The Low State (Max)	96mA
Junction Temperature (Tj)	
Ceramic	+175C
Thermal Resistance	
Junction-to-Case (Theta JC)	See Mil-Std 1835
Storage Temperature	-65C to +150C
Lead Temperature	
(Soldering, 10 seconds)	+300C
ESD Classification	Class 2
Maximum Power Dissipation	500 mW

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Supply Voltage (Vcc)	4.5V to 5.5V
Operating Temperature	-55C to +125C
Minimum Input Edge Rate (dV/dt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Maximum Output Current	
High Level (Ioh)	-24 mA
Low Level (Iol)	48 mA

## Electrical Characteristics

### DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICCH	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		1.0	mA	1, 2, 3
ICCL	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		68.0	mA	1, 2, 3
ICCZ	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		1.0	mA	1, 2, 3
ICCT	Supply Current per Input	VCC=5.5V Input under test=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		2.5	mA	1, 2, 3
IIH	High Level Input Current	VCC=5.5V, VINH=5.5V	1, 4	IN		5.0	uA	1, 2, 3
IIL	Low Level Input Current	VCC=5.5V, VINL=0.0V	1, 4	IN		-5.0	uA	1, 2, 3
IOZH	Maximum TRI-STATE Leakage Current HIGH	VCC=5.5V, For Control Inputs affecting output under test, Vin = 2.0V or 0.8V Vout = 2.7V	1, 4	OUT		50.0	uA	1, 2, 3
IOZL	Maximum TRI-STATE Leakage Current LOW	VCC=5.5V, For Control Inputs affecting output under test, Vin = 2.0V or 0.8V Vout = 0.5V	1, 4	OUT		-50.0	uA	1, 2, 3
ICEX	Output High Leakage Current	VCC=5.5V, VOUT=5.5V VINH=5.5V	1, 4	OUT		50.0	uA	1, 2, 3
IOS1 (Io)	Output Short Circuit Current	VCC=5.5V, VOUT=2.5V VINH=5.5V	1, 4, 10	OUT	-50	-180	mA	1, 2, 3
IBVI	Input High Current Breakdown Test	VCC=5.5V, VINH=7.0V	1, 4	IN		7.0	uA	1, 2, 3
IZZ (Ioff)	Bus Drainage Test	VCC=0.0V, VOUT=5.5V, VINL=0.0V	1, 4	IN/OUT	-100	100	uA	1, 2, 3
VOL	Low Level Output Voltage	VCC=4.5V, IOL=48.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT		0.55	V	1, 2, 3
VOH	High Level Output Voltage	VCC=4.5V, IOH=-24.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.0		V	1, 2, 3
		VCC=4.5V, IOH=-3mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.5		V	1, 2, 3
		VCC=5.0V, IOH=-3mA, VINH=5.0V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	3.0		V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IKL=-18mA, VINH=4.5V, VINL=0.0V	1, 4	IN		-1.2	V	1, 2, 3
VOLP	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		1.1	V	4
VOLV	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		-1.7	V	4

## Electrical Characteristics

### DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VOHP	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		1.5	V	4
VOHV	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	OUT		-0.90	V	4
CIN	Input Capacitance	VCC=0.0V	7	IN		10.5	pF	4
COUT	Output Capacitance	VCC=5.0V	7	OUT		15.0	pF	4

### AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC: CL=50pF RL=500 OHMS TRISE/TFALL = 3.0ns

tpLH1	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	A, B to B, A	1.0	5.5	ns	9
			2, 5	A, B to B, A	1.0	6.5	ns	10, 11
tpLH2	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	LEAB, BA to B, A	1.0	6.0	ns	9
			2, 5	LEAB, BA to B, A	1.0	7.0	ns	10, 11
tpLH3	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	/CLKAB, BA to B, A	1.0	6.5	ns	9
			2, 5	/CLKAB, BA to B, A	1.0	7.5	ns	10, 11
tpHL1	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	A, B to B, A	1.0	6.5	ns	9
			2, 5	A, B to B, A	1.0	7.0	ns	10, 11
tpHL2	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	LEAB, BA to B, A	1.0	6.8	ns	9
			2, 5	LEAB, BA to B, A	1.0	7.8	ns	10, 11
tpHL3	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	/CLKAB, BA to B, A	1.0	7.0	ns	9
			2, 5	/CLKAB, BA to B, A	1.0	8.0	ns	10, 11

## Electrical Characteristics

### AC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC: CL=50pF RL=500 OHMS TRISE/TFALL = 3.0ns

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpZL	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	OEAB, /O EBA to B,A	1.0	6.0	ns	9
			2, 5	OEAB, /O EBA to B,A	1.0	6.5	ns	10, 11
tpZH	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	OEAB, /O EBA to B.A	1.0	5.6	ns	9
			2, 5	OEAB, /O EBA to B.A	1.0	6.3	ns	10, 11
tpHZ	Output Disable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	OEAB, /O EBA to B,A	1.0	6.5	ns	9
			2, 5	OEAB, /O EBA to B,A	1.0	7.2	ns	10, 11
tpLZ	Output Disable Time	VCC=5.0 @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	OEAB, /O EBA to B,A	1.0	6.0	ns	9
			2, 5	OEAB, /O EBA to B,A	1.0	6.8	ns	10, 11
ts 1(H/L)	Setup Time HIGH or LOW	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A to /CLKAB	4.5		ns	9, 10, 11
ts 2(H/L)	Setup Time HIGH or LOW	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	B to /CLKBA	4.0		ns	9, 10, 11
ts 3(H/L)	Setup Time HIGH or LOW (/CLK High)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A,B to LEAB,BA	1.5		ns	9, 10, 11
ts 4(H/L)	Setup Time HIGH or LOW (/CLK Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A,B to LEAB,BA	4.5		ns	9, 10, 11
th 1(H/L)	Hold Time HIGH or LOW	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A to /CLKAB	0.0		ns	9, 10, 11
th 2(H/L)	Hold Time HIGH or LOW	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	B to /CLKBA	0.0		ns	9, 10, 11
th 3(H/L)	Hold Time HIGH or LOW (/CLK High)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A,B to LEAB,BA	1.5		ns	9, 10, 11
th 4(H/L)	Hold Time HIGH or LOW (/CLK Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	A,B to LEAB,BA	1.5		ns	9, 10, 11
tw (H/L)	Pulse Width	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	LEAB/BA, High	3.3		ns	9, 10, 11

## Electrical Characteristics

### AC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC: CL=50pF RL=500 OHMS TRISE/TFALL = 3.0ns

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tw (H/L)	Pulse Width(/CLKBA,BA,High or Low)	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	/CLKAB,BA	3.3		ns	9, 10, 11
Fmax	Max Clock Frequency	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	7	/CLKAB,BA		150	Mhz	9, 10, 11

Note 1: Screen tested 100% on each device at -55C, +25C & +125C Temp., Subgroups 1,2,3,7 & 8.

Note 2: Screen tested 100% on each device at -55C, +25C, and +125C temp., subgroups A9, A10, and A11.

Note 3: Screen tested 100% on each device at +25C temp. only, subgroup A9.

Note 4: Sample tested (Method 5005, Table 1) on each mfg. lot at +25C, +125C, & -55C temp. subgroups A1, 2, 3, 7 & 8.

Note 5: Sample tested (Method 5005, Table 1) on each mfg. Lot at +25C, +125C & -55C temp., subgroups A9, 10 & 11.

Note 6: Sample tested (Method 5005, Table 1) on each mfg. Lot at 25C temp only, subgroup A9.

Note 7: Not tested (Guaranteed by Design Characterization Data).

Note 8: Max number of outputs defines as (N). N-1 data inputs are driven 0V to 3V. one output @Vol or @Voh.

Note 9: Max number of data inputs (N) switching. (N-1) inputs switching 0V to 3.0V. Input-undertest switching: 3V to threshold(VILD), 0V to threshold(VIHD), Freq. = 1Mhz.

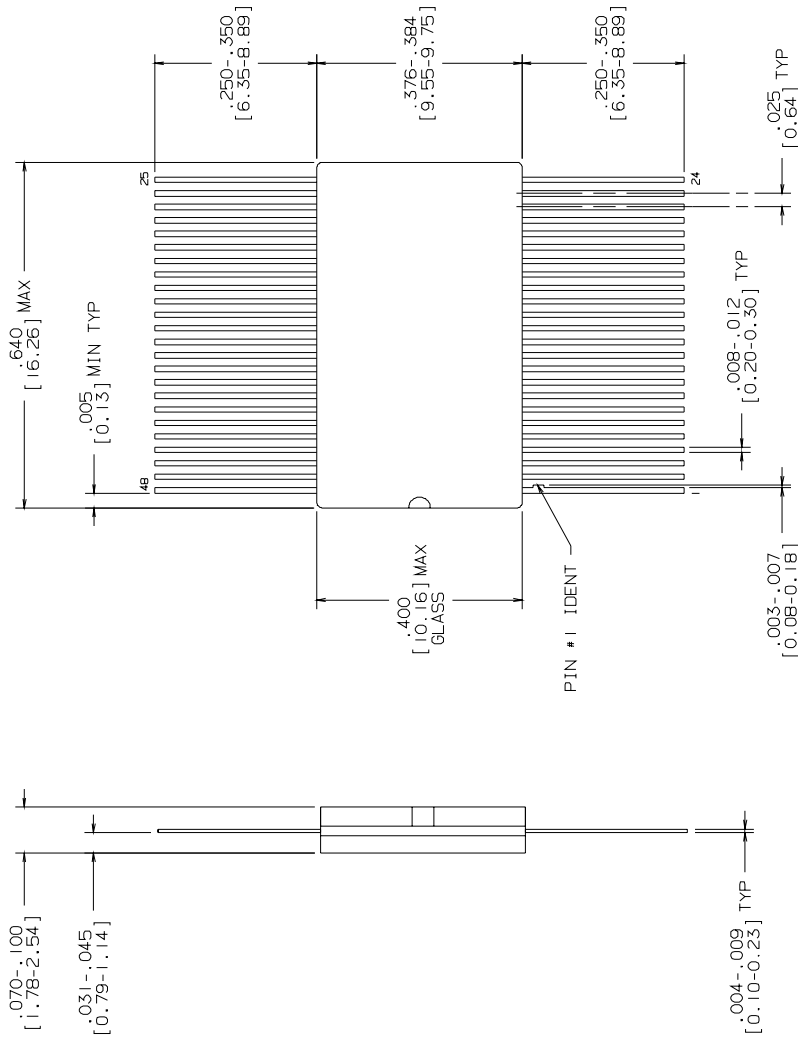
Note 10: Maximum test duration not to exceed one second, not more than one output shorted at one time.

### Graphics and Diagrams

GRAPHICS#	DESCRIPTION
WA48ARB	CERPAC, 48 LEAD, .025 LEAD PITCH (P/P DWG)

See attached graphics following this page.

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	09283	08/11/92
B	DIM .003-.007 [0.08-0.18] WAS .030-.045 [0.76-1.14] WAS .040-.054 [1.02-1.37]	09489	01/25/93
			M5/



MILAERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- STANDARD LEAD FINISH:  
200 MICRONS/5.08 MICROMETERS MINIMUM SOLDER  
MEASURED AT THE CREST OF THE MAJOR FLATS.
- THE LEAD FINISH, NICKEL UNDERPLATE, AND BASIS METAL  
SHALL CONFORM TO THE REQUIREMENTS OF MIL-M-38510.
- REFERENCE JEDEC METRIC BALLLOT JC-11.10-92-75, ITEM 10-320,  
VARIATION AA, DATED JULY 9, 1992.

CONTROLLING DIMENSION: INCH			
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DRAWN MARTA SUCHY	08/11/92	2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
DFG: CHK.		CERPAC, 48 LEAD, .025 LEAD PITCH	
ENGR. CHK.			
APPROVAL			
PROJECTION		SCALE	DRAWING NUMBER
		N/A	C MKT-WA48A
		DO NOT SCALE DRAWING	SHEET 1 OF 1
		REV	B

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0001551	07/08/97	Bill Petcher	Changed unit 'uA' to 'mA' in ICCH unit column of AC Parameters, due to incorrect entry(Type-0).