

MN54ACT112-X REV 2A0

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Dual JK Negative Edge-Triggered Flip-Flop

General Description

The ACT112 contain two Independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on \overline{SD} or \overline{Cd} prevents clocking and forces Q or \overline{Q} HIGH respectively. Simultaneous LOW signals on \overline{SD} and \overline{CD} force both Q or \overline{Q} HIGH.

Asynchronous Inputs

LOW input in \overline{SD} (Set) sets Q to HIGH level

LOW input to \overline{CD} (Clear) sets Q to LOW level

Clear and Set are independent of clock.

Simultaneous LOW on \overline{CD} and \overline{SD} makes both Q and \overline{Q} HIGH

Industry Part Number

54ACT112

NS Part Numbers

54ACT112DMQB
 54ACT112FMQB
 54ACT112LMQB

Prime Die

J112

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25 C
2	Static tests at	+125 C
3	Static tests at	-55 C
4	Dynamic tests at	+25 C
5	Dynamic tests at	+125 C
6	Dynamic tests at	-55 C
7	Functional tests at	+25 C
8A	Functional tests at	+125 C
8B	Functional tests at	-55 C
9	Switching tests at	+25 C
10	Switching tests at	+125 C
11	Switching tests at	-55 C

Features

- ACT112 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
- ACT112: 5962-89950

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.5V to +7.0V
DC Input Diode Current (Iik)	
Vi = -0.5V	-20 mA
Vi = Vcc +0.5V	+20 mA
DC Output Diode Current (Iok)	
Vo = -0.5V	-20 mA
Vo = Vcc +0.5V	+20 mA
DC Output Voltage (Vo)	-0.5V to Vcc +0.5V
DC Output Source or Sink Current (Io)	±50 mA
DC Vcc or Ground Current per Output Pin (Icc or Ignd)	±50 mA
Storage Temperature (Tstg)	-65 C to +150 C
Junction Temperature (Tj)	
CDIP	175 C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (Vcc)	4.5V to 5.5V
Input Voltage (Vi)	0V to Vcc
Output Voltage (Vo)	0V to Vcc
Operating Temperature (Ta)	-55 C to +125 C
Minimum Input Edge Rate (Delta V/Delta t)	
ACT Devices	
Vin From 0.8V to 2.0V	
Vcc @ 4.5V, 5.5V	125 mV/ns

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: VCC 4.5V to 5.5V, Temp. Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 3 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	High level input Current	VCC=5.5V, VIH=5.5V	1, 2	INPUT		0.1	uA	1
			1, 2	INPUT		1.0	uA	2, 3
IIL	Low level input Current	VCC=5.5V, VIL=0.0V	1, 2	INPUT		-0.1	uA	1
			1, 2	INPUT		-1.0	uA	2, 3
VOL	Low level output voltage	VCC=4.5V, VIL=0.8V, IOL=50.0uA, VIH=2.0V	1, 2	OUTPUT		.10	V	1, 2, 3
			1, 2	OUTPUT		.10	V	1, 2, 3
		VCC=4.5V, VIL=0.8V, IOL=24.0mA, VIH=2.0V	1, 2	OUTPUT		.36	V	1
			1, 2	OUTPUT		.50	V	2, 3
		VCC=5.5V, VIL=0.8V, IOL=24.0mA, VIH=2.0V	1, 2	OUTPUT		.36	V	1
			1, 2	OUTPUT		.50	V	2, 3
VIOL	Dynamic Output Current LOW	VCC=5.5V, VIH=5.5V, VIL=0.0V, IOL=50.0mA	1, 2, 5	OUTPUT		1.65	V	1, 2, 3
VOH	High level output voltage	VCC=4.5V, VIH=2.0V, VIL=0.8V, IOH=-50.0uA	1, 2	OUTPUT	4.40		V	1, 2, 3
			1, 2	OUTPUT	5.40		V	1, 2, 3
		VCC=4.5V, VIH=2.0V, VIL=0.8V, IOH=-24.0mA	1, 2	OUTPUT	3.86		V	1
			1, 2	OUTPUT	3.70		V	2, 3
		VCC=5.5V, VIH=2.0V, VIL=0.8V, IOH=-24.0mA	1, 2	OUTPUT	4.86		V	1
			1, 2	OUTPUT	4.70		V	2, 3
VIOH	Dynamic Output Current HIGH	VCC=5.5V, VIH=5.5V, VIL=0.0V, IOH=-50.0mA	1, 2, 5	OUTPUT	3.85		V	1, 2, 3
ICCH	Supply Current Outputs HIGH	VCC=5.5V, VIH=5.5V	1, 2	VCC		8.0	uA	1
			1, 2	VCC		160	uA	2, 3
ICCL	Supply Current Outputs LOW	VCC=5.5V, VIL=0.0V	1, 2	VCC		8.0	uA	1
			1, 2	VCC		160	uA	2, 3
ICCT	Supply Current per Input	VCC=5.5V, VINH=3.4V	1, 2	VCC		1.0	mA	1
			1, 2	VCC		1.6	mA	2, 3

Electrical Characteristics

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: CL=50pf, RL=500 OHMS, TRISE=3.0ns, TFALL=3.0ns, Temp Range: -55C to 125C. NOTE: -55C TEMPERATURE,
 SUBGROUP 11 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=4.5V	3, 4, 6	\overline{CPn} to Qn/ \overline{Qn}	2.5	13.0	ns	9
			3, 4, 6	\overline{CPn} to Qn/ \overline{Qn}	2.5	14.0	ns	10, 11
tpHL(1)	Propagation Delay	VCC=4.5V	3, 4, 6	\overline{CPn} to Qn/ \overline{Qn}	2.5	13.0	ns	9
			3, 4, 6	\overline{CPn} to Qn/ \overline{Qn}	2.5	14.0	ns	10, 11
tpLH(2)	Propagation Delay	VCC=4.5V	3, 4, 6	$\overline{CD}/\overline{SDn}$ -Qn/ \overline{Qn}	2.5	10.0	ns	9
			3, 4, 6	$\overline{CD}/\overline{SDn}$ -Qn/ \overline{Qn}	2.5	11.0	ns	10, 11
tpHL(2)	Propagation Delay	VCC=4.5V	3, 4, 6	$\overline{CD}/\overline{SDn}$ -Qn/ \overline{Qn}	2.5	12.5	ns	9
			3, 4, 6	$\overline{CD}/\overline{SDn}$ -Qn/ \overline{Qn}	2.5	13.5	ns	10, 11
Fmax	Maximum Clock Frequency	VCC=4.5V	3, 4	\overline{CPn}	95		MHz	9
			3, 4	\overline{CPn}	80		MHz	10, 11
tw(H/L)(1)	Pulse Width	VCC=4.5V	3, 4	\overline{CPn}	5.0		ns	9, 10, 11
tw(H/L)(2)	Pulse Width	VCC=4.5V	3, 4	$\overline{CDn}/\overline{SDn}$	5.0		ns	9, 10, 11
ts(H/L)	Setup Time HIGH or LOW	VCC=4.5V	3, 4	Jn/ \overline{Kn} to \overline{CPn}	7.0		ns	9
			3, 4	Jn/ \overline{Kn} to \overline{CPn}	8.0		ns	10, 11
th(H/L)	Hold Time HIGH or LOW	VCC=4.5V	3, 4	Jn/ \overline{Kn} to \overline{CPn}	1.5		ns	9, 10, 11
TREC	Recovery Time		3, 4	$\overline{CD}/\overline{SDn}$ to \overline{CPn}	3.0		ns	9, 10, 11

Note 1: SCREEN TESTED 100% ON EACH DEVICE AT +25C & +125C TEMPERATURE, SUBGROUPS 1, 2, 7, & 8.

Note 2: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A1, 2, 7 & 8.

Note 3: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMPERATURE ONLY, SUBGROUP A9.

Note 4: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A9 & 10.

Note 5: TRANSMISSION LINE DRIVING TEST, GUARDBANDED LIMITS SET FOR +25C, 2 MSEC DURATION MAX.

Note 6: +25C & +125C MIN LIMITS GUARANTEED FOR 5.5 BY GUARDBANDING 4.5V MINIMUM LIMITS.